What is claimed is:

1. A semiconductor apparatus comprising:

a signal providing circuit which provides an input signal set including at least one input signal;

a data analyzer outputting a digital result signal in synchronization with a clock signal;

wherein said data analyzer inverts said digital result signal at a timing indicated by said clock signal while said input signal set is in a predetermined state, and does not invert said digital result signal while said input signal set is not in said predetermined state.

2. The semiconductor apparatus according to claim 1, wherein said input signal set includes first and second digital signals, and said predetermined state is a coincident state in which said first and second digital signal coincide with each other.

3. The semiconductor apparatus according to claim 1, wherein said data analyzer includes:

a logic circuit outputting a flip-flop input signal in response to said input signal set, and

a flip-flop latching said flip-flop input

signal to store a storage datum, and outputting said digital result signal in response to said storage datum, and

said logic circuit outputs said flip-flop input signal so as to appear an inverse of said storage datum while said input signal set is in a predetermined state, and outputs said flip-flop input signal so as to indicate said storage datum while said input signal set is not in a predetermined state.

4. The semiconductor apparatus according to claim 3, wherein said at least one input signal is digital, and said logic circuit comprises:

an inverter which receives said storage datum and outputs an inverted signal indicative of an inverse of said storage datum, and

an exclusive OR gate outputting said flip-flop input signal so as to indicate an exclusive OR of said at least on input signal and said inverted signal.

5. A semiconductor apparatus comprising:

a set of n comparators which is responsive to 2n input signals for outputting n digital result signals, wherein an i-th comparator (i being an natural number not more than n) of said

n comparator is responsive to a (2i-1)-th input signal and a 2i-th input signal of said 2n input signals for outputting an i-th digital result signal of said n digital result signals in synchronization with a clock signal; and

an OR gate outputting a total result signal indicative of an OR of said n digital result signals, wherein

said i-th comparator inverts said i-th digital result signal at a timing indicated by said clock signal while said (2i-1)-th input signal and said 2i-th input signal coincide with each other, and does not invert said digital result signal while said (2i-1)-th input signal and said 2i-th input signal do not coincide with each other.

6. A semiconductor apparatus comprising:

a set of n comparators which is responsive to 2n input signals for outputting n digital result signals, wherein an i-th comparator (i being an natural number not more than n) of said n comparator is responsive to a (2i-1)-th input signal and a 2i-th input signal of said 2n input signals for outputting an i-th digital result signal of said n digital result signals in synchronization with a clock signal; and

10725035.053960

an AND gate outputting a total result signal indicative of an AND of said n digital result signals, wherein

said i-th comparator inverts said i-th digital result signal at a timing indicated by said clock signal while said (2i-1)-th input signal and said 2i-th input signal coincide with each other, and does not invert said digital result signal while said (2i-1)-th input signal and said 2i-th input signal do not coincide with each other.

7. A semiconductor apparatus comprising:

an address generator which provides a tested memory with an address;

a test pattern generator which provides said test memory with a test pattern to have an access to said address, and generates an expected pattern expected to be outputted from said tested memory;

a comparator which compares an output pattern from said tested memory with said expected pattern to output a digital result signal in synchronization with a clock signal;

wherein said comparator inverts said digital result signal at a timing indicated by said clock signal while said output pattern coincides with

said expected pattern, and does not invert said digital result signal while said output pattern does not coincide with said expected pattern.

8. The semiconductor apparatus according to claim 7, wherein said tested memory and said semiconductor apparatus are embedded in a single semiconductor chip.

9. A semiconductor apparatus comprising:

a plurality of test circuits, each of which includes:

an address generator which provides a tested memory with an address,

a test pattern generator which provides said test memory with a test pattern to have an access to said address, and generates an expected pattern expected to be outputted from said tested memory, and

a comparator which compares an output pattern from said tested memory with said expected pattern to output a digital result signal in synchronization with a clock signal, said comparator inverting said digital result signal at a timing indicated by said clock signal while said output pattern coincides with said expected pattern, and not inverting said digital

result signal while said output pattern does not coincide with said expected pattern; and

an OR gate outputting a total result signal indicative of an OR of said digital result signal.

10. The semiconductor apparatus according to claim 9, wherein said tested memory and said semiconductor apparatus are embedded in a single semiconductor chip.

11. A semiconductor apparatus comprising:

a plurality of test circuits, each of which includes:

an address generator which provides a tested memory with an address,

a test pattern generator which provides said test memory with a test pattern to have an access to said address, and generates an expected pattern expected to be outputted from said tested memory, and

a comparator which compares an output pattern from said tested memory with said expected pattern to output a digital result signal in synchronization with a clock signal, said comparator inverting said digital result signal at a timing indicated by said clock signal while said output pattern coincides with said

expected pattern, and not inverting said digital result signal while said output pattern does not coincide with said expected pattern; and

an AND gate outputting a total result signal indicative of an AND of said digital result signal.

12. The semiconductor apparatus according to claim 11, wherein said tested memory and said semiconductor apparatus are embedded in a single semiconductor chip.

13. A method of operating a semiconductor apparatus, comprising:

providing an input signal set including at least one input signal;

outputting a digital result signal in response to said input signal set in synchronization with a clock signal; wherein said digital result signal is inverted at a timing indicated by said clock signal while said input signal set is in a predetermined state, and is not inverted while said input signal set is not in said predetermined state.

14. A method of testing a circuit, comprising:

inputting an output pattern from said

circuit to a semiconductor apparatus;

inputting an expected pattern to said semiconductor apparatus, said expected pattern being expected to be outputted from said circuit;

inputting a clock signal to said semiconductor apparatus;

outputting a digital result signal by said semiconductor apparatus in response to said output pattern and said expected pattern in synchronization with said clock signal, wherein said digital result signal is inverted at a timing indicated by said clock signal while said output pattern coincides with said expected pattern, and is not inverted while said output pattern does not coincide with said expected pattern.